What is claimed:

1. A method for manufacturing a semiconductor device, the method comprising the steps of:

(a) forming a gate dielectric layer on a semiconductor layer;

(b) forming a first conduction layer having a specified pattern on the gate dielectric layer;

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(c) forming sidewall insulation layers on side walls of the first conduction layer;

(d) forming a source region and a drain region in the semiconductor layer;

(e) depositing a first insulation layer that covers the first conduction layer and the sidewall insulation layers, the first insulation layer comprising a material different from that of the sidewall insulation layers;

(f) planarizing the first insulation layer until an upper surface of the first conduction layer is exposed;

(g) removing a part of the first conduction layer in a manner that the gate dielectric layer is not exposed to thereby form a recessed section on the first conduction layer between the sidewall insulation layers;

(h) partially filling a second conduction layer in the recessed section to form a gate electrode that includes at least the first conduction layer and the second conduction layer;

(i) forming a second insulation layer at the recessed section on the second conduction layer, the second insulation layer being composed of a material different from that of the first insulation layer;

(j) etching the first insulation layer to form a first through hole that reaches the source region or the drain region; and

(k) forming a first contact layer in the first through hole.

2. A method for manufacturing a semiconductor device according to claim 1, wherein, in the step (j), the second insulation layer and the sidewall insulation layers are composed of a material that is more difficult to etch than the first insulation layer.

3. A method for manufacturing a semiconductor device according to claim 1, wherein the first conduction layer is a silicon layer, and the step (h) includes the steps of

(h – 1) depositing a metal layer for siliciding the first conduction layer on the first conduction layer; and

(h – 2) siliciding the first conduction layer to form a silicide layer.

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4. A method for manufacturing a semiconductor device according to claim 1, further comprising:

(l) forming a third insulation layer on the first insulation layer and the second insulation layer;

(m) etching the third insulation layer to form a second through hole; and

(n) forming a second contact layer in the second through hole, wherein the first through hole is continuous to the second through hole.

5. A method for manufacturing a semiconductor device according to claim 1, wherein, in the step (j), the second insulation layer is formed from a material having a ratio of an etching rate of the second insulation layer with respect to an etching rate of the first insulation layer being two or greater.

6. A method for manufacturing a semiconductor device according to claim 1, wherein the first insulation layer comprises silicon oxide and the second insulation layer comprises silicon nitride.

7. A method for manufacturing a semiconductor device according to claim 1, wherein, in the step (j), the sidewall insulation layers are formed from a material having a ratio of an etching rate of the sidewall insulation layers with respect to an etching rate of the first insulation layer being two or greater.

8. A method for manufacturing a semiconductor device according to claim 1, wherein the first insulation layer comprises silicon oxide and the sidewall insulation layers comprise silicon nitride.

9. A method for manufacturing a semiconductor device, comprising:

forming a gate dielectric layer on a semiconductor layer;

forming a first conduction layer having a specified pattern on the gate dielectric layer;

forming sidewall insulation layers on side walls of the first conduction layer;

forming a source region and a drain region in the semiconductor layer;

removing a part of the first conduction layer in a manner so that the gate dielectric layer is not exposed, to thereby form a recessed section on the first conduction layer between the sidewall insulation layers, wherein the removing a part of the first conduction layer is carried out after formation of the source region and the drain region;

forming a second conduction layer in a portion of the recessed section; and

forming an insulation layer in the recessed section on the second conduction layer.

10. A method for manufacturing a semiconductor device according to claim 9, further comprising, after forming the source region and the drain region and before removing a part of the first conduction layer:

forming a first insulating layer that covers the first conduction layer, the sidewall insulation layers, and the semiconductor layer; and

planarizing the first insulation layer so that the first conduction layer is exposed.

11. A method for manufacturing a semiconductor device according to claim 10, further comprising, after forming the insulation layer in the recessed section above the second conduction layer:

etching the first insulation layer to form a first through hole that reaches the source region or the drain region; and

forming a first contact layer in the first through hole.

12. A method for manufacturing a semiconductor device according to claim 9, wherein the second conducting layer comprises a silicide.

13. A method for manufacturing a semiconductor device according to claim 9, wherein the removing a part of the first conduction layer further includes removing a greater depth of the first conduction layer from a center region than from end regions adjacent to the sidewall insulation layers.

14. A semiconductor device including a field effect transistor, the field effect transistor including a gate dielectric layer, a gate electrode, a source region and a drain region, comprising:

a second insulation layer formed on the gate electrode;

sidewall insulation layers formed on side walls of the gate electrode;

a first insulation layer formed on the sides of sidewall insulation layers,

the gate electrode including a first conduction layer and a second conduction layer,

the first conduction layer being formed on the gate dielectric layer,

the second conduction layer being formed above the first conduction layer;

a first through hole reaching the source region or the drain region formed in the first insulation layer; and

a first contact layer formed in the first through hole,

wherein, as the thickness of the first conduction layer is compared based on a top surface of the gate dielectric layer, the first conduction layer has thickness that gradually becomes greater from a central section thereof toward the side walls thereof.

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15. A semiconductor device including a field effect transistor, the field effect transistor including a gate dielectric layer, a gate electrode, a source region and a drain region, comprising:

a second insulation layer formed on the gate electrode;

sidewall insulation layers formed on side walls of the gate electrode;

a first insulation layer formed on the sides of sidewall insulation layers,

the gate electrode including a first conduction layer and a second conduction layer,

the first conduction layer being formed on the gate dielectric layer,

the second conduction layer being formed above the first conduction layer;

a first through hole reaching the source region or the drain region formed in the first insulation layer;

a first contact layer formed in the first through hole,

wherein, as the thickness of the first conduction layer is compared based on a top surface of the gate dielectric layer, an end portion of the first conduction layer has a greater thickness as compared to a thickness thereof at a central section thereof.

16. A semiconductor device according to claim 14, wherein, as the height of an upper surface of the second conduction layer is compared based on an upper surface of the gate dielectric layer, the height of the upper surface of the second conduction layer gradually becomes higher from a central section thereof toward the side walls.

17. A semiconductor device according to claim 15, wherein, as the height of an upper surface of the second conduction layer is compared based on an upper surface of the gate dielectric layer, the height of the upper surface of the second conduction layer at the side wall sections thereof is higher than a height of the upper surface of a central section thereof.

18. A semiconductor device according to any one of claim 15, wherein the second conduction layer comprises a material selected from the group consisting of a metal, a metal alloy and a metal compound.

19. A semiconductor device according to claim 15, wherein the first conduction layer is a silicon layer, and the second conduction layer is a silicide layer.

20. A semiconductor device according to claim 15, further comprising:

a third insulation layer formed on the first insulation layer and the second insulation layer;

a second through hole formed in the third insulation layer, being continuous with the first through hole; and

a second contact layer formed in the second through hole.

21. A semiconductor device according to any one of claim 15, wherein the first insulation layer is formed from silicon oxide, and the second insulation layer is formed from silicon nitride.

22. A semiconductor device according claim 15, wherein the first insulation layer is formed from silicon oxide, and the sidewall insulation layers are formed from silicon nitride.

23. A semiconductor device according claim 15, wherein the upper surface of the first insulation layer and the upper surface of the second insulation layer are substantially at the same level.